

# United States Patent and Trademark Office

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,982 09/17/2003		David Chong Sook Lim	112055-0040P1	4640
24267 7.	590 03/28/2006	EXAMINER		
CESARI AND MCKENNA, LLP 88 BLACK FALCON AVENUE			ANDUJAR, LEONARDO	
BOSTON, MA			ART UNIT	PAPER NUMBER
ŕ			2826	·
			DATE MAILED: 03/28/200	6

Please find below and/or attached an Office communication concerning this application or proceeding.

V	f
Ĭ	

		Application No.	Applicant(s)				
Office Action Summary		10/664,982	LIM ET AL.				
		Examiner	Art Unit				
		Leonardo Andújar	2826				
The MAILING DATE of this com Period for Reply	munication appe	ars on the cover sheet with the c	orrespondence add	lress			
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.  - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.  - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).							
Status							
1) Responsive to communication(s	) filed on <u>21 Feb</u>	oruary 2006.					
2a) This action is FINAL.	☐ This action is <b>FINAL</b> . 2b) ☑ This action is non-final.						
3) Since this application is in condi		·		merits is			
closed in accordance with the p	ractice under Ex	parte Quayle, 1935 C.D. 11, 45	3 O.G. 213.				
Disposition of Claims							
4) Claim(s) <u>1,3-5,7 and 8</u> is/are pe	nding in the app	lication.					
4a) Of the above claim(s)	is/are withdrawn	n from consideration.					
5) Claim(s) is/are allowed.							
6)⊠ Claim(s) <u>1,3-5,7 and 8</u> is/are rej							
7) Claim(s) is/are objected t		alastian raquirament					
8) Claim(s) are subject to re	estriction and/or	election requirement.					
Application Papers							
9)☐ The specification is objected to b	·						
10) The drawing(s) filed on is.	•						
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).							
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.							
The oath of declaration is object	ed to by the Exa	miner. Note the attached Office	Action of form F iv	<i>9</i> -132.			
Priority under 35 U.S.C. § 119							
<ul> <li>12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).</li> <li>a) All b) Some * c) None of:</li> <li>1. Certified copies of the priority documents have been received.</li> <li>2. Certified copies of the priority documents have been received in Application No.</li> <li>3. Copies of the certified copies of the priority documents have been received in this National Stage</li> </ul>							
application from the International Bureau (PCT Rule 17.2(a)).							
* See the attached detailed Office a	action for a list o	f the certified copies not receive	d.				
Attachment(s)							
1) Notice of References Cited (PTO-892)  4) Interview Summary (PTO-413)  2) Paper No(s)/Mail Date							
Paper No(s)/Mail Date  Notice of Draftsperson's Patent Drawing Review (PTO-948)  Paper No(s)/Mail Date  Notice of Informal Patent Application (PTO-152)  Paper No(s)/Mail Date  Other:							

### **DETAILED ACTION**

### Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 01/31/2006 has been entered.

### Election/Restrictions

2. Applicant's election without traverse of species 1 (fig. 3) in the reply filed on 03/24/2005 is acknowledged.

## Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

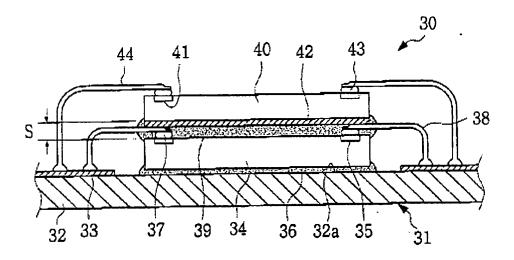
A person shall be entitled to a patent unless -

- (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
- 4. Claims 1, 3, 5 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Kang et al. (US 2003/017810 A1).
- 5. Regarding claim 1 Kang (e.g. fig. 3) shows a die containing package comprising: a die 34 defining electrical die contacts 35, a substrate 31 defining first substrate

Art Unit: 2826

6.

contacts (i.e. the contact/pad areas defined by 33/38), flattened electrical conductive balls 37 attached to the die contacts and making electrical connection thereto, electrical conductive runs 33 on the substrate 12 connecting the first substrate contacts to second substrate contacts (i.e. the contact/pad areas defined by 33/44), electrically conductive wires 38 with first ends making electrical connections to the first substrate contacts, wherein the wires are formed to run substantially parallel to the surface of the die and wherein the other ends are horizontally attached to the flattened balls.



- 7. Regarding claim 3, Kang shows that the second substrate contacts are located on the substrate opposite the first substrate contacts (e.g. right side vs. left side).
- 8. Regarding claim 5, Kang (e.g. fig. 3) shows process for packaging a die comprising the steps of: defining electrical die contacts 35, defining a substrate 31 with first substrate contacts (i.e. the contact/pad areas defined by 33/38); flattening an electrical conductive balls 37, attaching the flattened electrically conductive balls to the die contacts, forming electrical conductive runs 33 on the substrate 31 connecting the first substrate contacts to second substrate contacts (i.e. the contact/pad areas defined

by 33/44), connecting electrically conductive wires 38 to the first substrate contacts, running the electrically conductive wires substantially parallel to the surface of the die contacts and horizontally attaching the other ends of the wires to the flattened electrically conductive balls thereby making electrical connections therebetween and whereon the other ends remain substantially parallel to the surface of the die.

9. Regarding claim 7, Shim shows that the second substrate contacts are located on the substrate opposite the first substrate contacts (right side vs. left side).

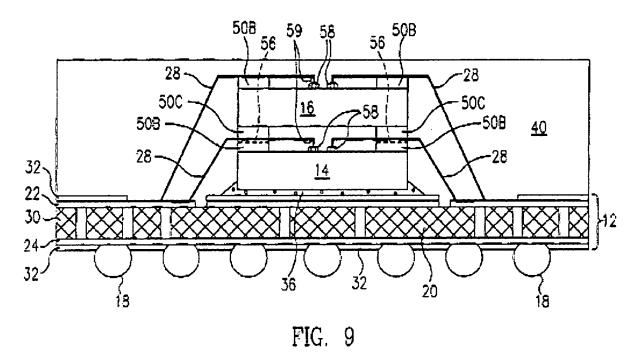
## Claim Rejections - 35 USC § 103

- 10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
  - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 11. Claims 1, 3-5, 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shim et al. (US 6,531,784) in view of Kang et al. (US 2003/017810 A1).
- 12. Regarding claim 1 Shim (e.g. fig. 9) shows a die containing package comprising: a die 14 defining electrical die contacts, a substrate defining first substrate contacts, flattened electrical conductive balls 58 attached to the die contacts and making electrical connections thereto, electrical conductive runs 22/24 on the substrate 12 connecting the first substrate contacts (i.e. the electrical contacts formed by the runs and the wires 28) to second substrate contacts 18, electrically conductive wires 28 with a first ends making electrical connection to the first substrate contacts, and wherein the

Application/Control Number: 10/664,982

Art Unit: 2826

other ends are arranged making electrical connections to the flattened electrical conductive balls attached to the die contacts.



Shim does not teach that other ends are horizontally attached to the flattened ball. Nevertheless, Kang (e.g. fig. 3) shows electrically conductive wires 38 that run substantially parallel to the surface of the die and have ends that are horizontally attached to flattened balls 37. According to Kang, this type of connection minimizes a space between the first chip and a second chip, thereby reducing the total height of the semiconductor stack (abstract). It would have been obvious to one of ordinary skill in the art at the time the invention was made to horizontally attach the other ends of the wires disclosed by Shim to the fattened balls in accordance to Kang's invention to minimize the space between the first and the second chip, thereby reducing the total height of the semiconductor stack.

Art Unit: 2826

- 13. Regarding claim 3, Shim shows that the second substrate contacts are located on the substrate opposite the first substrate contacts.
- 14. Regarding claim 4, Shim shows that the second substrate contacts are located to accommodate a pin out different from the die.
- 15. Regarding claim 5. Shim (e.g. fig. 9) shows process for packaging a die comprising the steps of: defining electrical die contacts, defining a substrate 12 with first substrate contacts, flattening an electrical conductive balls 58, attaching the flattened electrically conductive balls to the die contacts, forming electrical conductive runs 22/24 on the substrate 12 connecting the first substrate contacts (i.e. the electrical contacts formed by the runs and the wires 28) to second substrate contacts 18, connecting electrically conductive wires 28 to the first substrate contacts, running the electrically conductive wires substantially parallel to the surface of the die contacts and attaching the other ends of the wires to the flattened electrically conductive balls thereby making electrical connections therebetween and wherein the other ends remain substantially parallel to the surface of the die. Shim does not teach that other ends are horizontally attached to the flattened ball. Nevertheless, Kang (e.g. fig. 3) shows electrically conductive wires 38 that run substantially parallel to the surface of the die and have ends that are horizontally attached to flattened balls 37. According to Kang, this type of connection minimizes a space between the first chip and a second chip, thereby reducing the total height of the semiconductor stack (abstract). It would have been obvious to one of ordinary skill in the art at the time the invention was made to horizontally attach the other ends of the wires disclosed by Shim to the fattened balls in

Art Unit: 2826

accordance to Kang's invention to minimize the space between the first and the second chip, thereby reducing the total height of the semiconductor stack.

- 16. Regarding claim 7, Shim shows that the second substrate contacts are located on the substrate opposite the first substrate contacts.
- 17. Regarding claim 8, Shim shows that the second substrate contacts are located to accommodate a pin out 18 different from the die.

### Response to Arguments

18. Applicant's arguments filed 01/31/2006 have been fully considered but they are most in view of new grounds of rejection.

### Conclusion

- 19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonardo Andújar whose telephone number is 571-272-1912. The examiner can normally be reached on Mon through Thu from 9:00 AM to 7:30 PM EST.
- 20. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.
- 21. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

Application/Control Number: 10/664,982

Art Unit: 2826

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

Leonardo Anduja Primary Examiner Art Unit 2826 Page 8